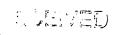


Electronic Filing System (EFS) Data **Electronic Patent Application Submission**



JUL 27 2004

USPTO Use Only

TECH CENTER 2011

EFS ID:

65085

Application ID:

09972011

Method and arrangement for

layout and manufacture of

Title of Invention:

nonmanhattan semiconductor

integrated circuit using

simulated euclidean wiring

First Named Inventor:

Steven Teig

Domestic/Foreign Application:

Domestic Application

Filing Date:

2001-10-05

Effective Receipt Date:

2004-07-22

Submission Type:

Information Disclosure

Statement

Filing Type:

Confirmation number:

5250

Attorney Docket Number:

SPLX.P0068

Total Fees Authorized:

180.0

Payment Category:

Credit Card

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08312004

Card Holder Name:

Mani Adeli

Postal Code:

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RAM Payment Status:

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RAM User ID:

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RAM Accounting Date:

2004-07-22

RAM Sequence Number:

1084080

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Electronic Version v1.1 Stylesheet Version v1.1.0

UL 27 2004

TIFCH CENTER 900

Title of Invention

Method and arrangement for layout and manufacture of nonmanhattan semiconductor integrated circuit using simulated euclidean wiring

Application Number:

09/972011

Date:

2001-10-05

First Named Applicant:

Steven Teig

Confirmation Number:

5250

Attorney Docket Number: SPLX.P0068

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Submitted by:	Elec. Sign.	Sign. Capacity
Mani Adeli Registered Number: 39,585	/Mani Adeli/	Attorney

Documents being submitted Files

us-fee-sheet SPLX.P0068-usfees.xml

us-fee-sheet.xsl

us-fee-sheet.dtd

us-ids SPLX.P0068-usidst.xml

us-ids.dtd

us-ids.xsl

Comments

This Information Disclosure Statement is submitted after receipt of a first Office Action on the merits but before the Final Office Action. Accordingly, a fee is required. The requisite fee is included with this electronic submission of the Information Disclosure Statement. Applicants hereby request that the one submitted fee be accepted for the second and any subsequent submission.

APP_ID=09972011 Page 2 of 2



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TRANSFECTIONIC Version v08 Stylesheet Version v08.0

TECH CENTER 2800

Title of Invention Method and arrangement for layout and manufacture of nonmanhattan semiconductor integrated circuit using simulated euclidean wiring

Application Number:

09/972011

Date:

2001-10-05

First Named Applicant:

Steven Teig

Attorney Docket Number: SPLX.P0068

Art Unit:

2825

Examiner:

Helen B. Rossoshek

TOTAL FEE AUTHORIZED \$180

Patent fees are subject to annual revisions on or about October 1st of each year.

BASIC FILING FEE

Fee Description	Fee Code	Amount \$	Fee Paid \$
Submission Of Information Disclosure Stmt Fee	1806	180	180

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ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18 Stylesheet Version v18.0

> Title of Invention

Method and arrangement for layout and manufacture of nonmanhattan semiconductor integrated circuit using simulated euclidean wiring

Application Number:

09/972011

Confirmation Number:

5250

First Named Applicant:

Steven Teig

Attorney Docket Number: SPLX.P0068

Art Unit:

2825

Examiner:

Helen B. Rossoshek

Search string:

(4855253 or 5541005 or 5635736 or 5637920 or 5640327 or 5646830 or 5650653 or 5689433 or 5723908 or 5784289 or 5801385 or 5811863 or 5822214 or 5880969 or 5889329 or 5980093 or 6150193 or 6260183 or 6262487 or 6263475 or 6301686 or 6307256 or 6316838 or 6324674

or 6412097 or 6448591 or 6516455 or 20010009031 or 20030025205).pn.

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Note: Applicant is not required to submit a paper copy of cited US Patent Documents

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	2	5541005	1996-07-30	Bezama et al.			
	3	5635736	1997-06-03	Funaki et al.			
	4	5637920	1997-06-10	Loo			
	5	5640327	1997-06-17	Ting			
	6	5646830	1997-07-08	Nagano			
	7	5650653	1997-07-22	Rostoker et al.			
	8	5689433	1997-11-18	Edwards			
	9	5723908	1998-03-03	Fuchida et al.			
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	27	6516455	2003-02-04	Teig et al.	B1

US Published Applications

Note: Applicant is not required to submit a paper copy of cited US Published Applications

init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
	1	20010009031	2001-07-19	Nitta et al.	A1		
	2	20030025205	2003-02-06	Shively	A1		

Signature

Examiner Name	Date		